22nm HP Integrated Patterning Improvements for EUVL

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SEMATECH EUV Focus Areas 2005-2009: 22 nm half-pitch insertion target*

2005 / 32hp	2006 / 32hp	2007 / 22hp**	2008 / 22hp	2009 / 22hp
1. Resist resolution, sensitivity & LER met simultaneously	1. Reliable high power source & collector module	1. Reliable high power source & collector module	1. Long-term source operation with 100 W at IF and 5MJ/day	1. Mask yield & defect inspection/review infrastructure
2. Collector lifetime	2. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Defect free masks through lifecycle & inspection/review infrastructure	2. Long-term reliable source operation with 200 W at IF
3. Availability of defect free mask	3. Availability of defect free mask	3. Availability of defect free mask	3. Resist resolution, sensitivity & LER met simultaneously	3. Resist resolution, sensitivity & LER met simultaneously
4. Source power	4. Reticle protection during storage, handling and use	4. Reticle protection during storage, handling and use	• Reticle protection during storage, handling and use	• EUVL manufacturing integration
▪ Reticle protection during storage, handling and use	5. Projection and illuminator optics quality & lifetime	5. Projection and illuminator optics quality & lifetime	• Projection / illuminator optics and mask lifetime	
▪ Projection and illuminator optics quality & lifetime				

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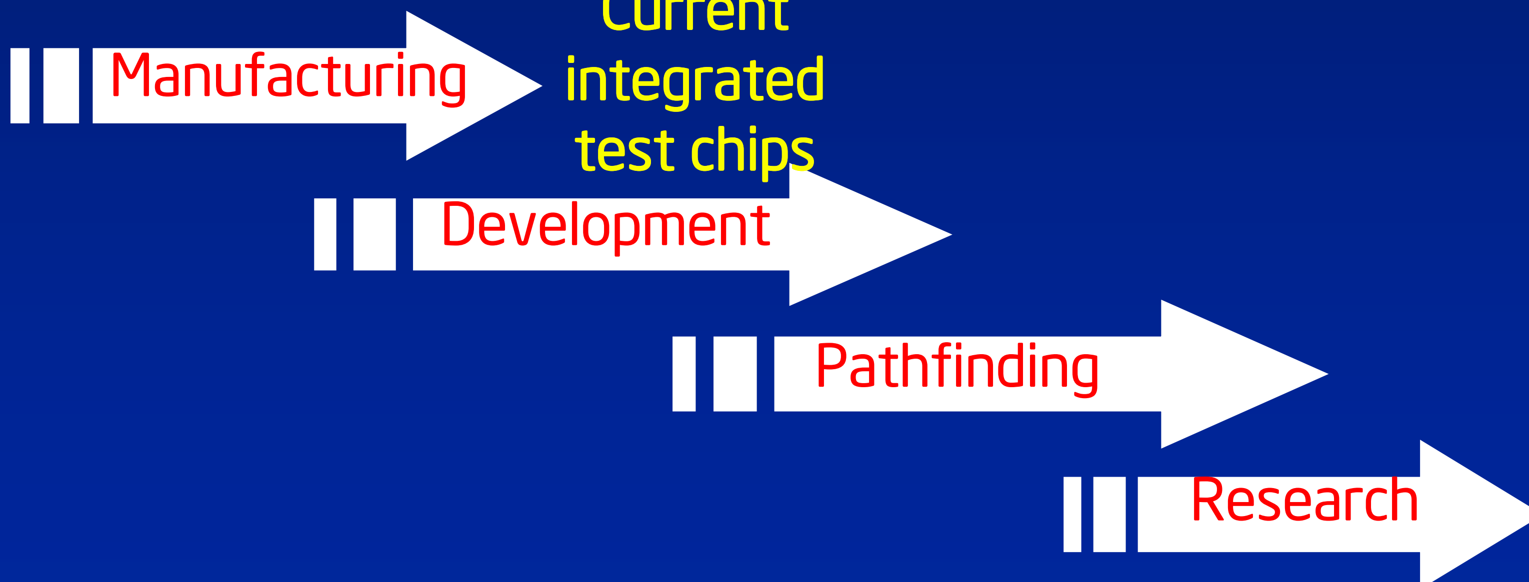
*2009 EUVL Symposium, SEMATECH

** 2007 focus was still 32 nm hp

Logic Technology Nodes

Process Name	P1266	P1268	P1270	P1272	P1274
1st Production	2007	2009	2011	2013	2015
Logic Tech. node*	45 nm	32 nm	22 nm	15 nm	11 nm

Current integrated test chips



* Logic technology node has no correspondence to half pitch

Intel's 11nm Node - 2015 HVM*

193i with Pitch Division can and will be extended as viable option for Intel's 11nm Node patterning in 2015

	32nm	22nm	15nm	11nm
Min Pitch	112.5nm	*0.71	*0.71	*0.71 = 40nm

Still Single Pitch Division, might need 5 masks for complex dense 2D layouts.

***ITRS 2008 Reference*:**

Year of Production	2013	2015	2017	2019	2021
MPU Metal 1 Pitch *nm*	64	50	40	31.8	25.2

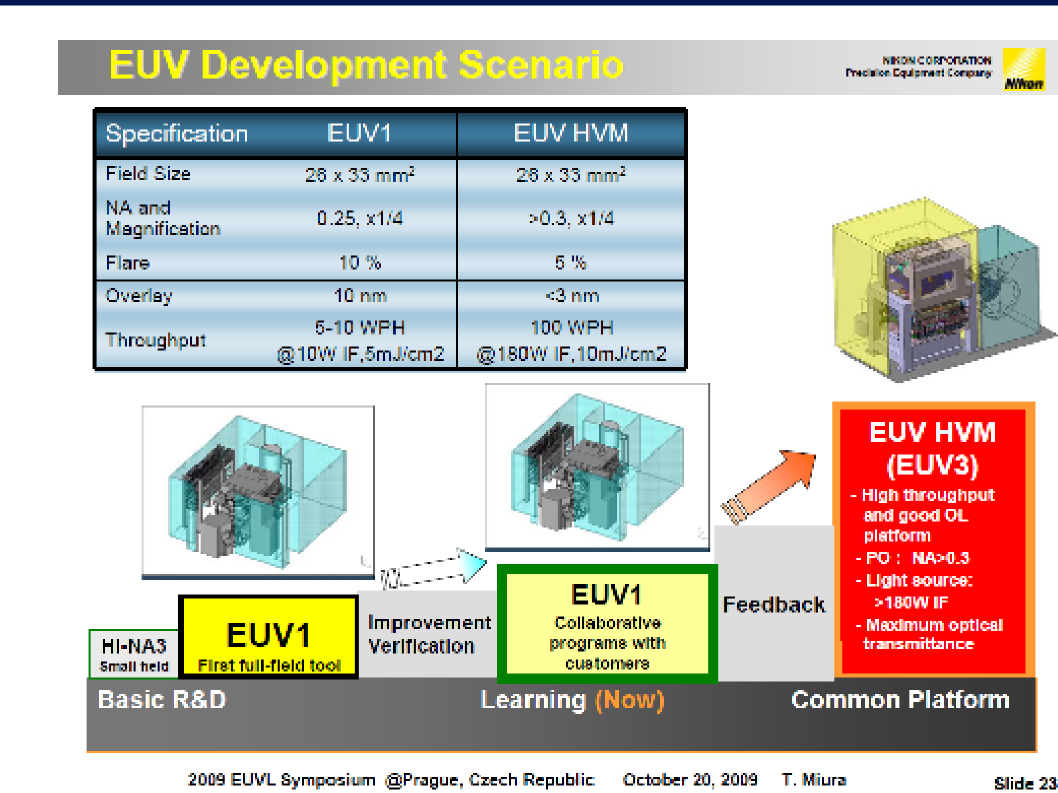
***Y. Borodovsky, Intel Corporation, 2009 SEMICON West**

Outline

What do we need to address 22 nm hp integrated process development using EUVL?

- Tools
- Resist
- Compensations

EUV HVM tool roadmaps have higher NA



"ASML EUV Program: Status and Prospects", J. Benschop, 2009 EUVL Symposium

"Nikon EUVL Development Progress Update", T. Miura, 2009 EUVL Symposium

- 0.3X NA tools are planned for HVM
- <u>Though initial development will be done with 0.25 NA tools</u>

EUV exposure tools: MET, EUV1, ADT**

Intel MET

Process transfer →

EUV1

IMEC ADT

0.25 NA resolution concerns for 22 nm hp

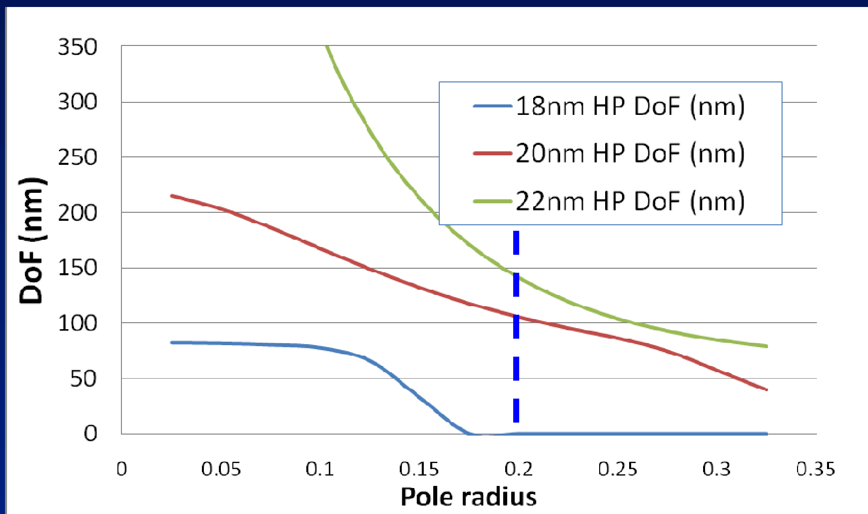
	Intel MET	Nikon EUV1	ADT
Field size	600 x 600 μm^2	26 x 33 mm^2	26 x 33 mm^2
NA	0.30*	0.25	0.25
Illumination	0.36/0.55 annular	0.5-0.8 sigma + OAI	0.5 disk
Flare	~7%	~12%	~16%
Overlay	No	Yes	Yes

*with 10% area central obscuration

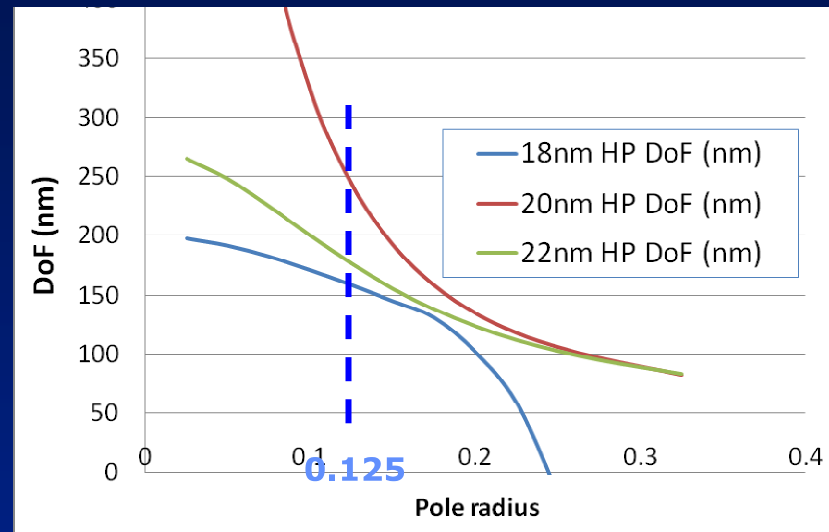
** G. Vandentop, SPIE 2009

How to squeeze the most out of 0.25 NA tools?

Dipole Center=0.60



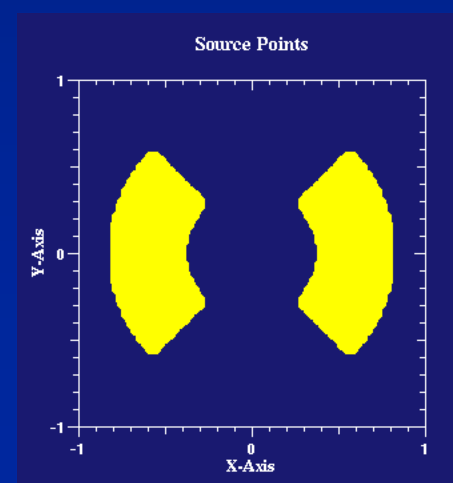
Dipole center=0.675



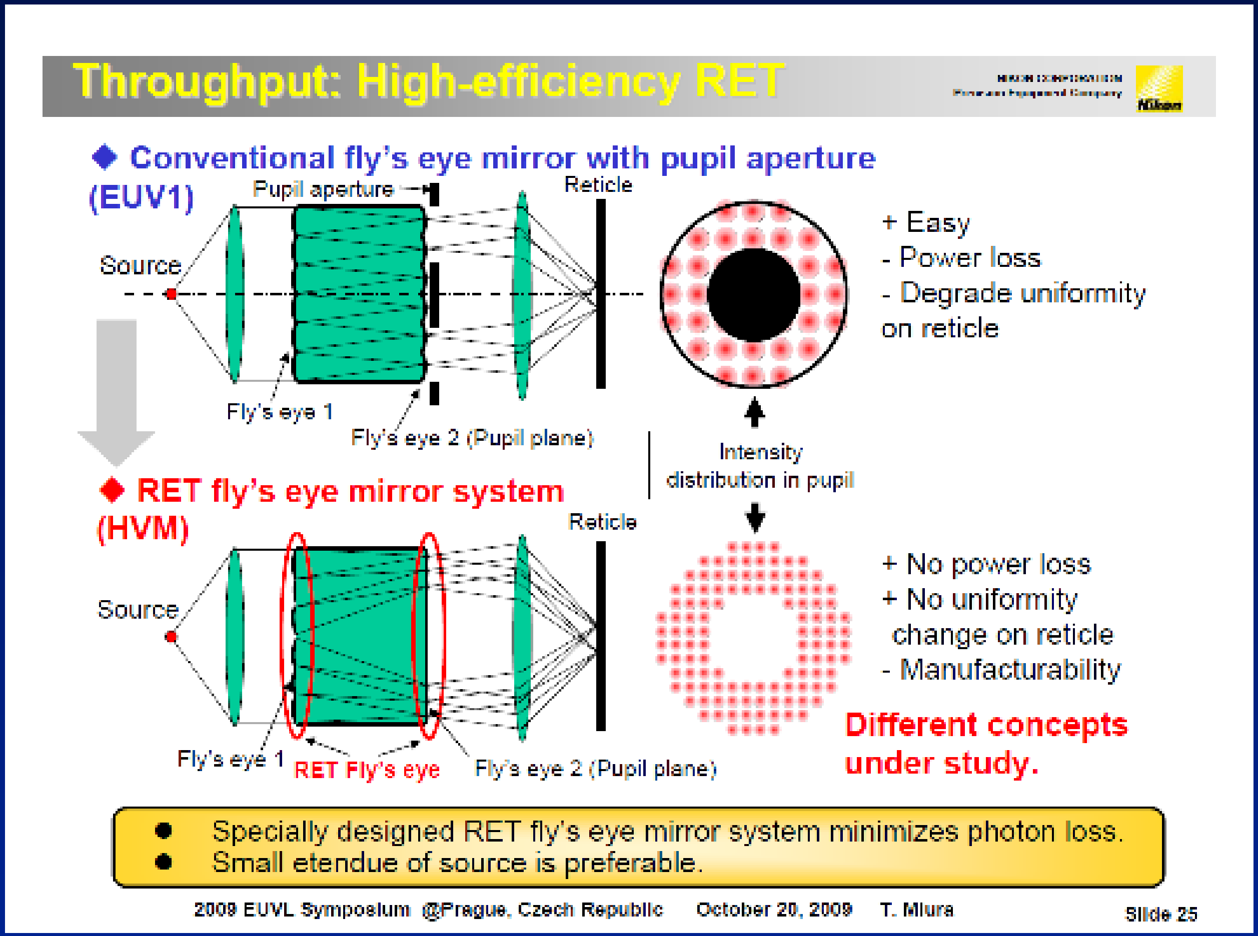
$\sigma_{max} \leq 0.8$

$$P\_opt = \frac{\lambda}{2 * P * NA}$$

- Aerial image modeling of line/space patterns
- DoF based on contrast > 60%
- Optimum pole center for < 22nm HP = 0.675
- Dipole angle optimized for throughput



High efficiency illuminators



"Nikon EUVL Development Progress Update", T. Miura, 2009 EUVL Symposium

- HVM systems will be equipped with high efficiency off axis illuminators that minimize throughput loss
- DR for P1274 will be set in Q3'2012 using 0.25 NA tools
- So, 0.32 NA designs need to match the OAI settings w 0.25 NA to carry forward the early development

Photoresist

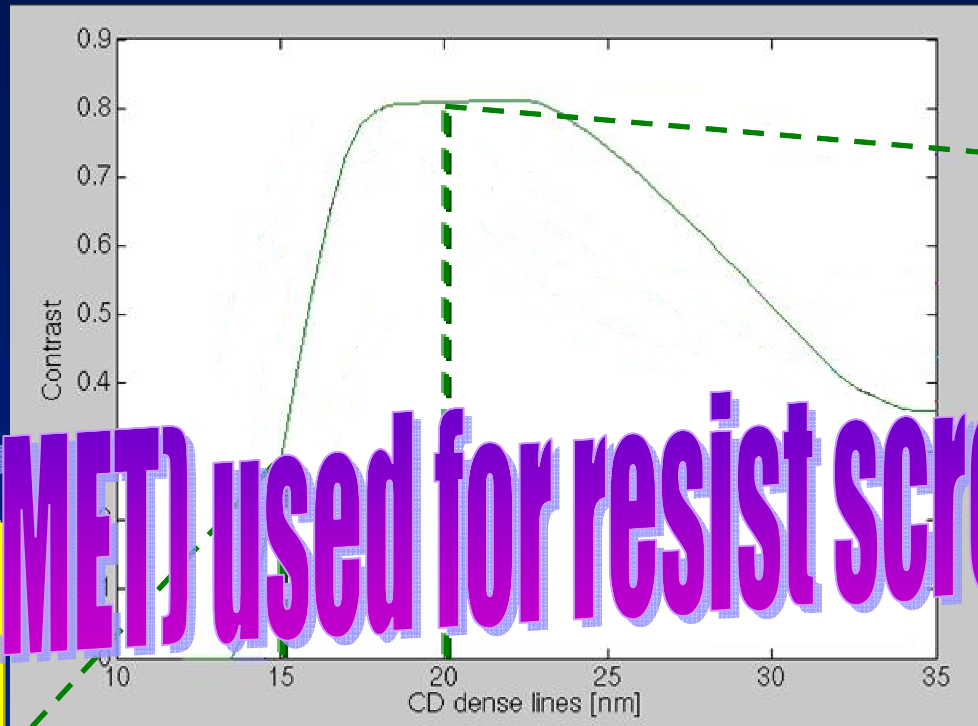
- Current capability
- LWR reduction
- Esize improvements
- 2D needs
- Contacts

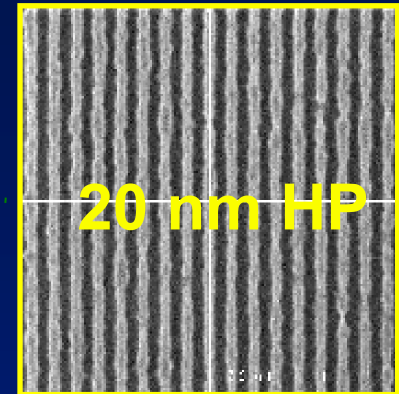
MET Aerial Image with OAD Capable of Modulation to 18nm HP :: Resist G*

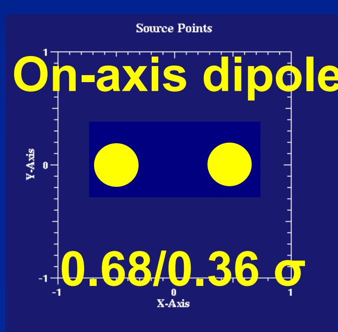
- **nZ_{22} = 35.1**
- Intel MET on-axis dipole capable of probing to 17 nm HP
- Contrast falls off at ≤ 17 nm HP

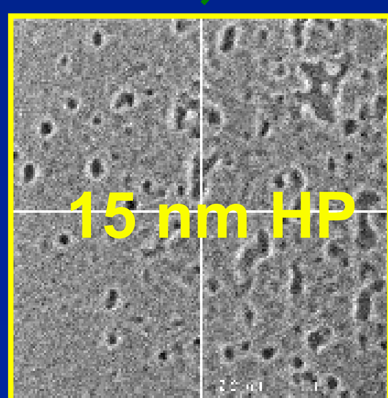
Higher NA tool (MET) used for resist screening

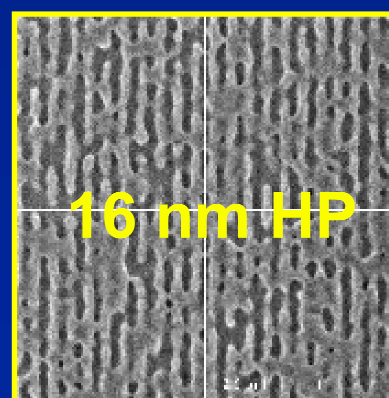
fronts

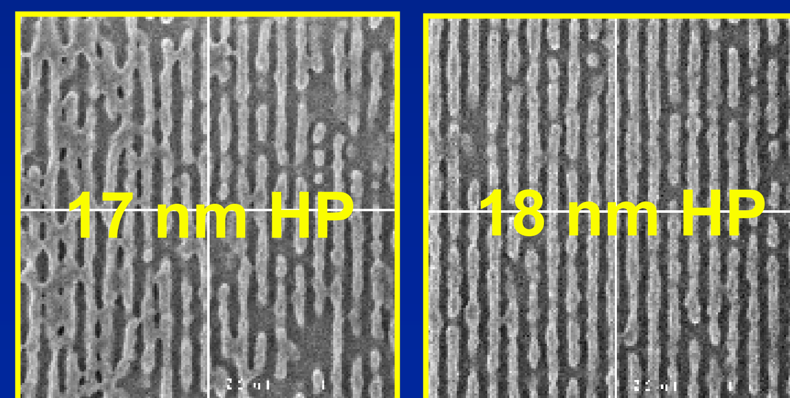










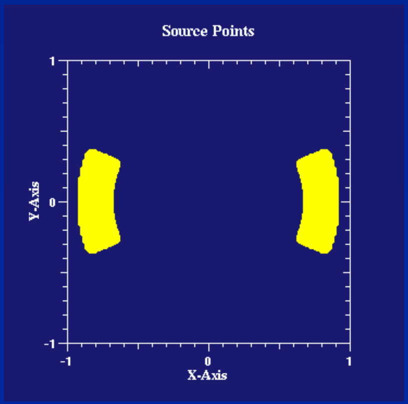


*T. Younkin, Intel Corporation, 2009 EUVL Symposium

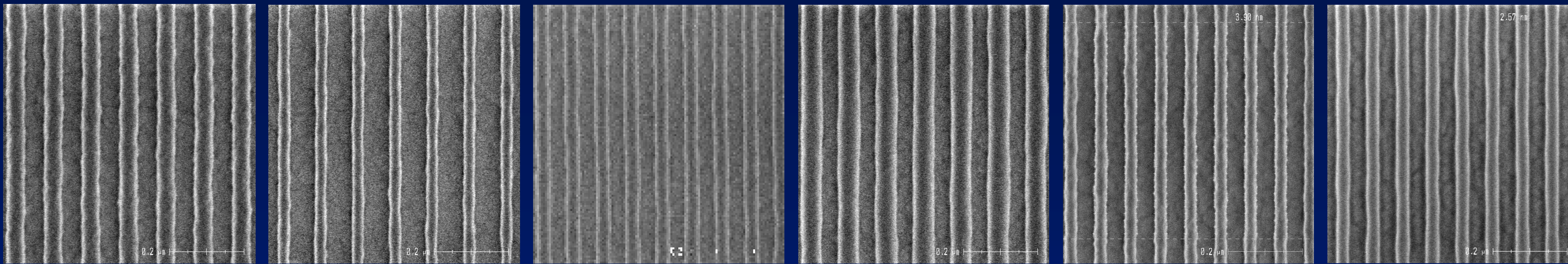
MET upgrades

- METs need to have better resolution than next generation full-field tools
- Current Intel MET has 0.3 NA with the potential upgrade path:
  - Outer sigma: 0.68 → 0.9 (~ 14 nm hp)
  - NA: 0.3 → 0.5 (~ 9 nm hp)

Ultimate resolution using dipole illumination



LWR Reduction Techniques*



No Treatment | Etch/Trim | Vapor Smoothing | Hardbake | Ozonation | Rinse

Explored Several Techniques with Leading EUV Platform

- **Physical (Etch/Trim, Hardbake)**
  - **–Photoresist chemistry independent**
- **Chemical (Vapor, Ozonation, Rinse Agent)**
  - **–Photoresist chemistry dependent**
- **Techniques that reduce LWR by ≥ 20% are worth pursuing**

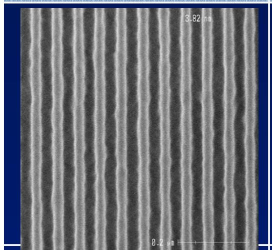
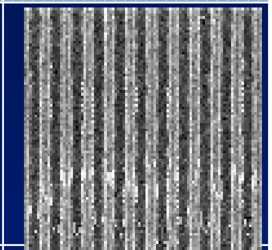
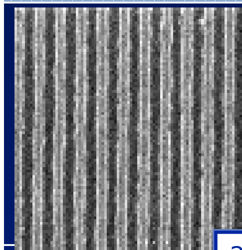
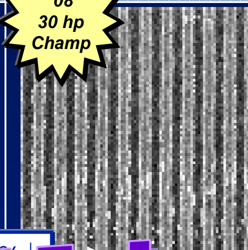
Technique	LWR reduction (nm)	%LWR reduction
Etch/Trim	0.5	10
Vapor smoothing	0.9	18
Hardbake	0.6	12
Ozonation	0.5	10
Rinse	2.0	40

Largest Improvement Observed using Rinse Agent

*Chandhok *et al*, J. Vac. Sci. Technol. B, (Nov 2008)

Photoresist improvements Year over Year

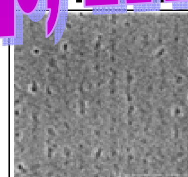
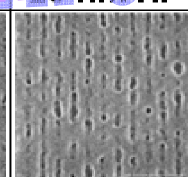
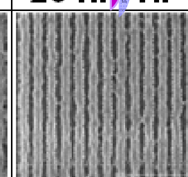
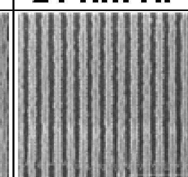
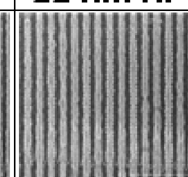
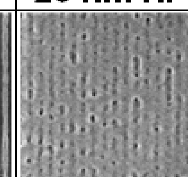
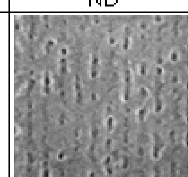
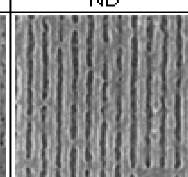
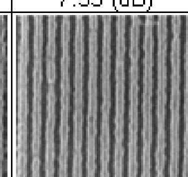
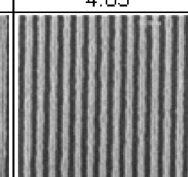
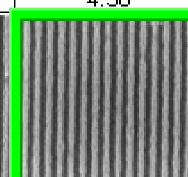
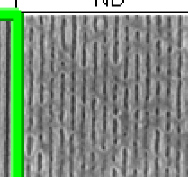
2008

30 nm HP	2008 "Smooth" RLS Champs		"Fast" RLS Champion	
	UL A + Resist C	UL A + Resist D	UL B + Resist E	UL B + Resist E Rinse 1
				'08 30 hp Champ 
MIN LWR (nm)	3.8	4.3	[illegible]3	3.[illegible]
DOSE [illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

28%↓

2010 target: 22 nm hp, LWR 3 nm, 11.3 mJ Esize

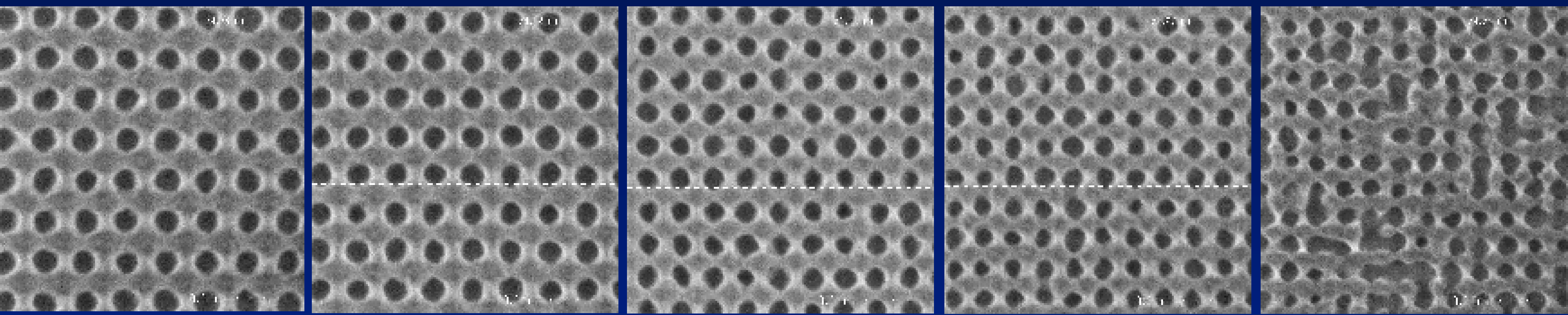
2009

	[illegible] nm HP	[illegible] nm HP	2[illegible] nm HP	24 nm HP	22 nm HP	20 nm HP
Resist F No Rinse						
Dose	12.70	12.70	12.70	12.70	12.70	12.70
LWR	ND	ND	7.35 (uB)	4.63	4.36	ND
Resist F Rinse 1						
Dose	12.80	12.80	12.80	12.80	12.80	12.80
LWR	ND	ND	6.20	4.90	4.27	ND

- Photoresist challenges of meeting Resolution, Linewidth roughness, and Sensitivity simultaneously being met with clever resist design and rinse

Contact Performance, Limited OPC
Quad Illumination, Intel-MET

30 nm hp | 28 nm hp | 24 nm hp | 22 nm hp | 20 nm hp



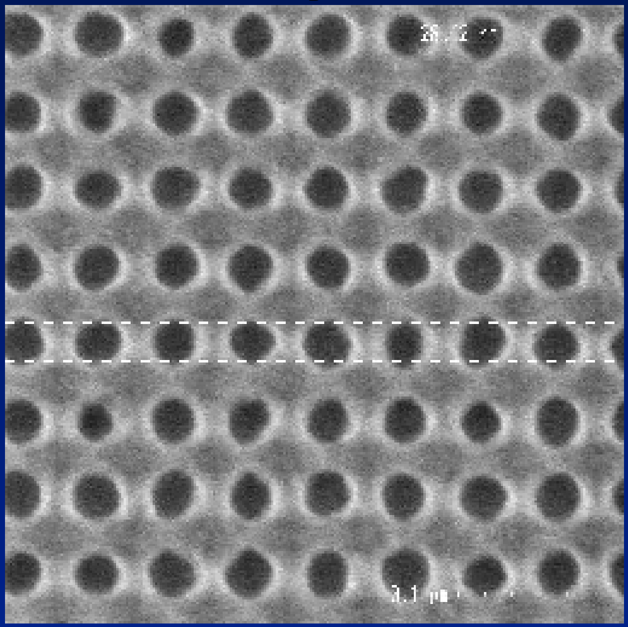
Resist R on UL A
FT = 50 nm

- Print bias ~8 nm (oversized contacts)

Good UR (~ 26 hp), but high Esize (22.5 mJ/cm^2)

intel

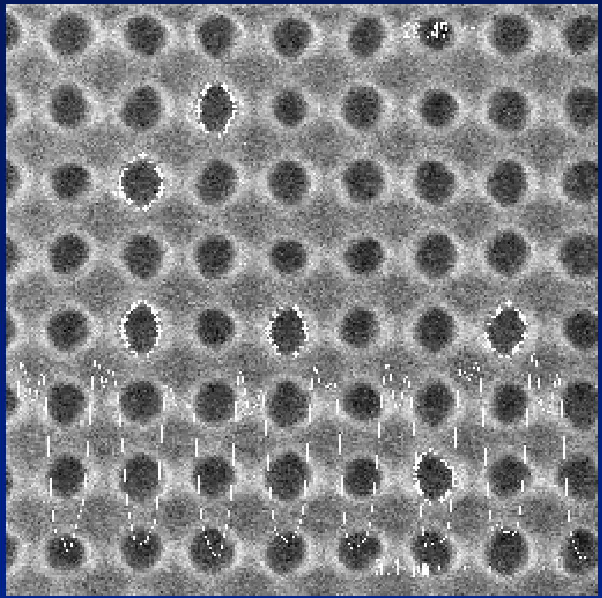
28 nm hp Contact resolution (gridded layout)



Resist R

FT = 50 nm

Esize = 22.5 mJ/cm^2



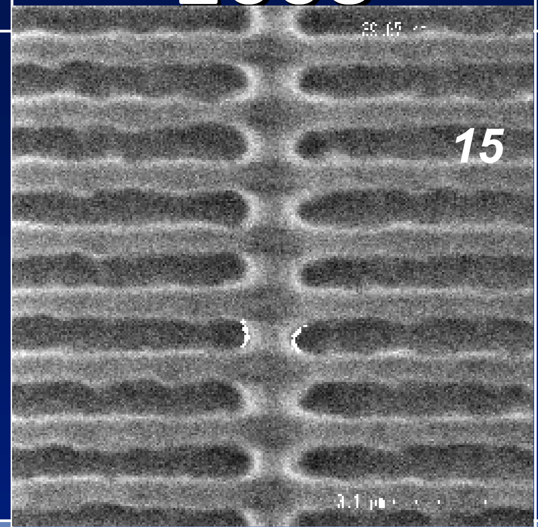
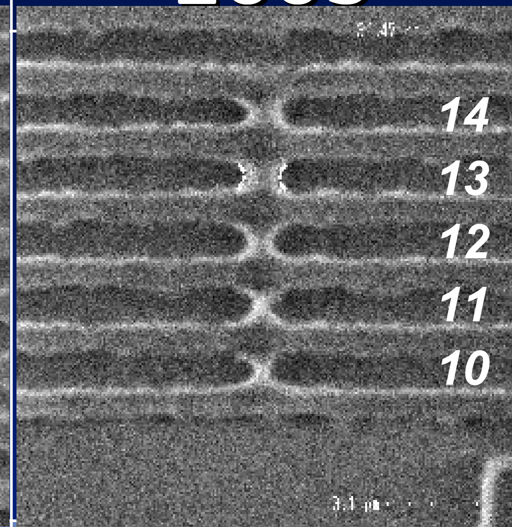
Resist F

FT = 50 nm

Esize = 13.75 mJ/cm^2

- Print bias ~8 nm (oversized contacts)
- Resist F has 30% better Esize than Resist R

2D / ETE Performance :: Progress

	2007	2008	2009
	Not Resolved ≤ 30 hp		
Resist	Resist S	Resist D	Resist K
Feature	30 nm hp	30 nm hp	30 nm hp
Min ETE	ND	40 nm	25 nm

- 2D local MEEF for uncorrected features BMs well against nZ improvements, validating screening methodology.

DR Restrictions and/or OPC Improvements Needed to Meet Aggressive Layer Targets

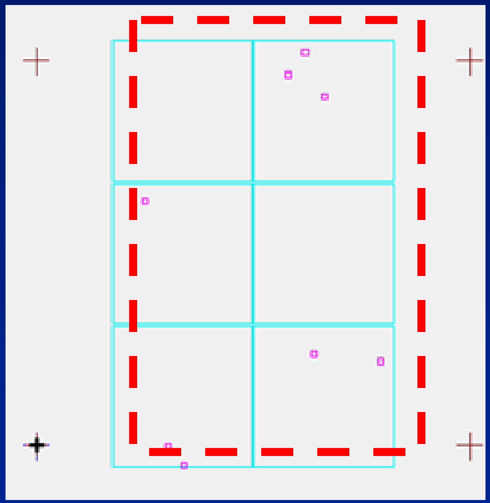
30 hp MEEF	nZ(32)
1.20	7.2
1.40	7.4
2.01	7.9
2.50	9.5

EUV Compensations

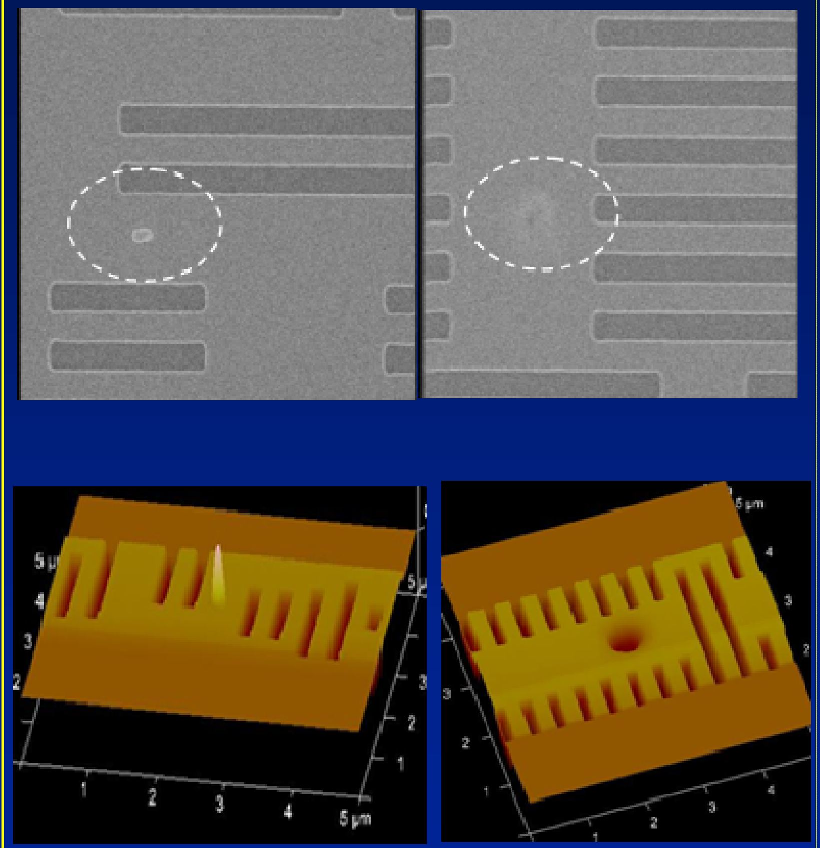
- Defect mitigation
- Flare induced CD variation
- Non-flatness induced overlay error
- HV bias shadowing
- OPC

Defect mitigation for large un-repairable defects

Defect mitigation by pattern shift

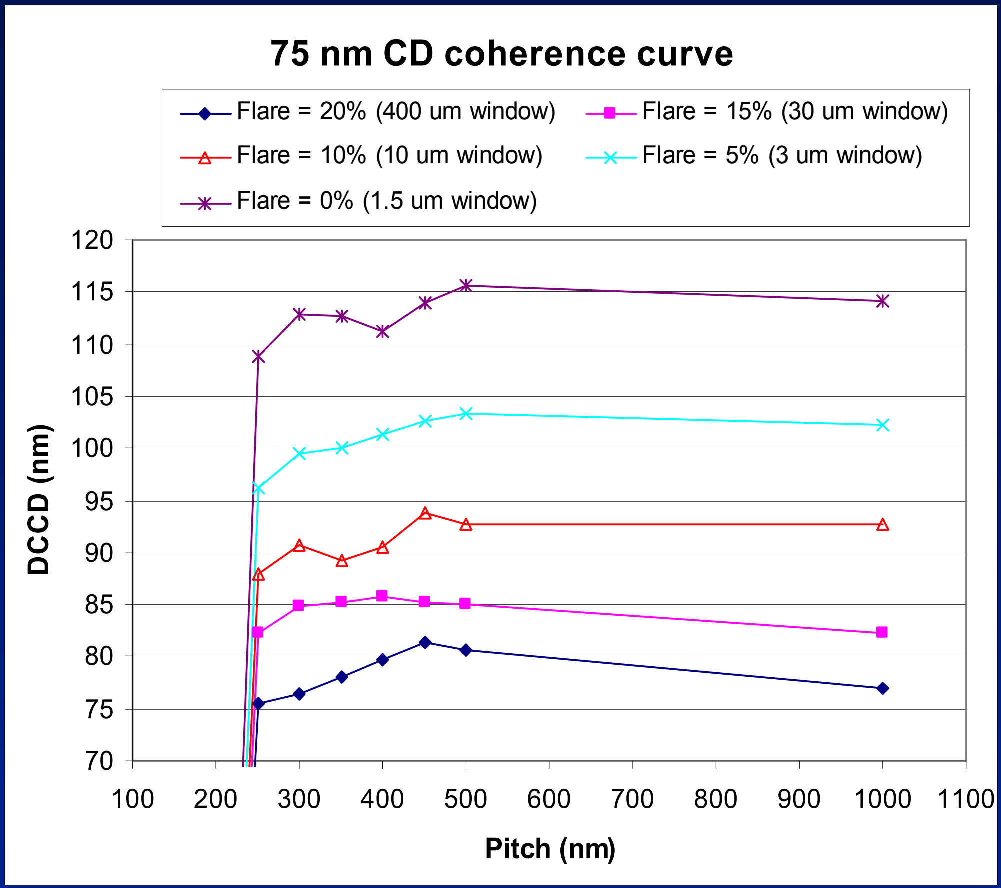


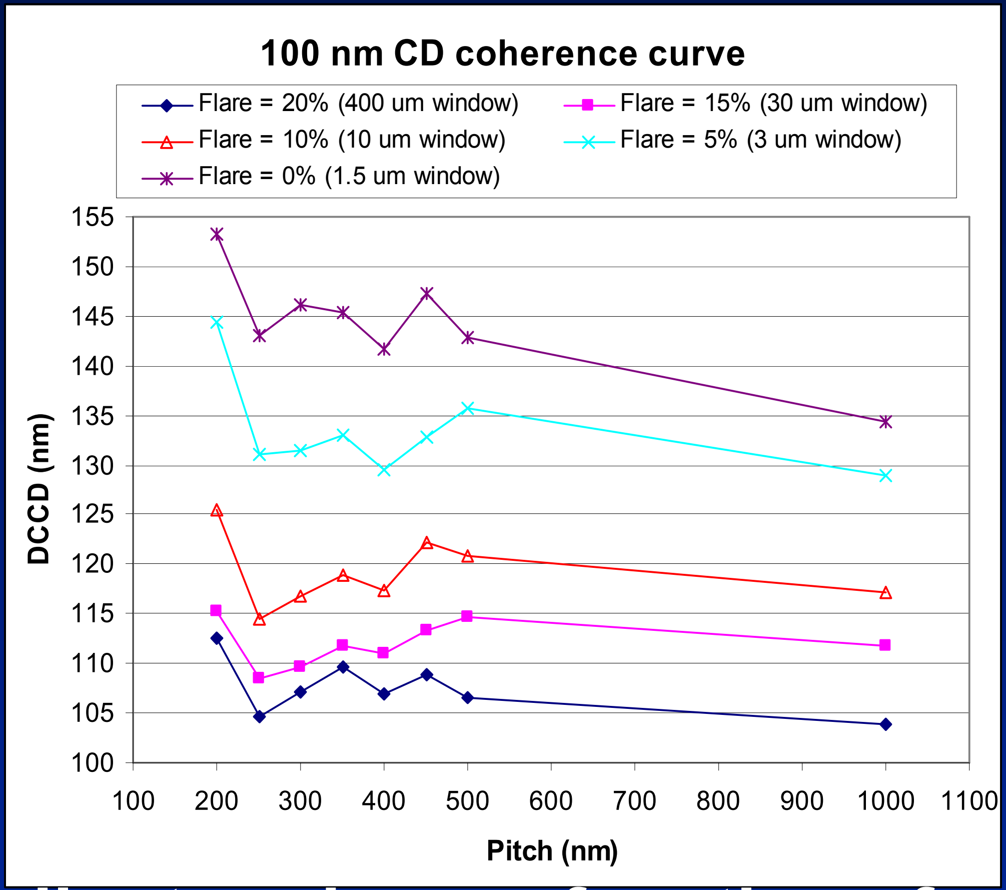
Note: Defects shown below are repairable



- Pattern shift calculated based on location within the field such that printable un-repairable defects are under large absorber areas
- Needs fiducial mark for reference

Flare Variation Compensation (FVC)*



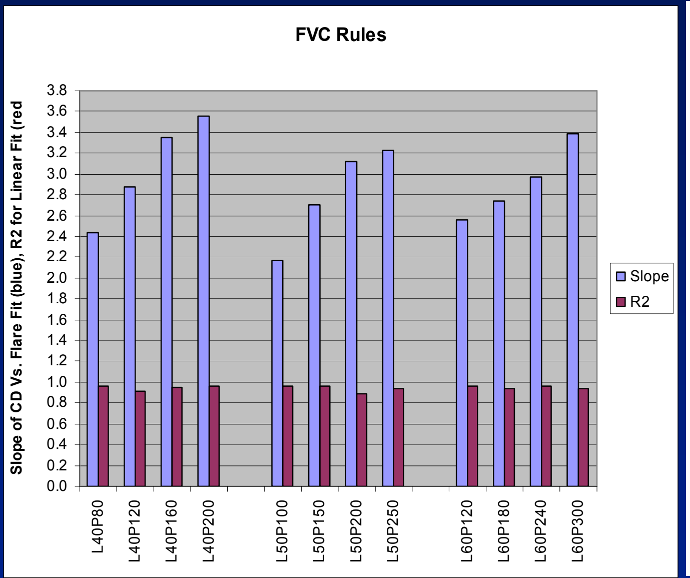


- Coherence curves have similar trends as a function of flare
- To 1st order, OPC can potentially be de-coupled from Flare Variation Compensation (FVC)

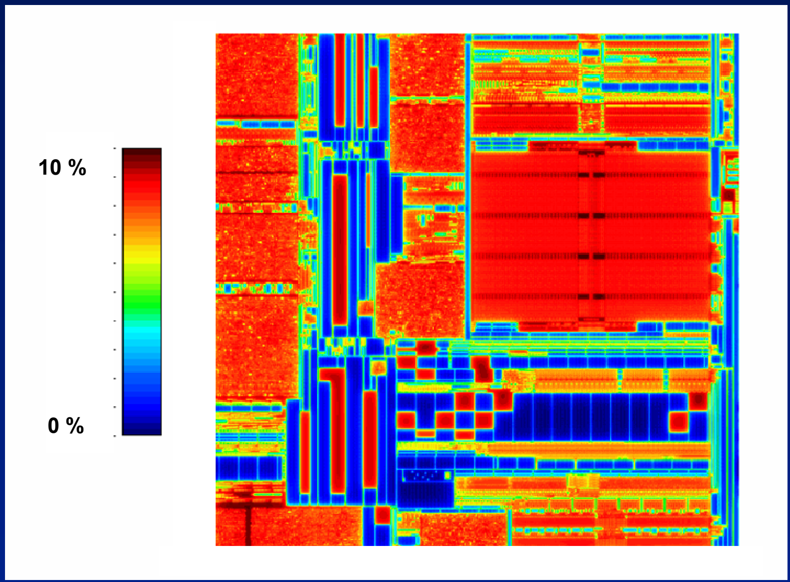
*M. Chandhok, SPIE 2004

FVC (Flare Variation Compensation) – test result on mask design

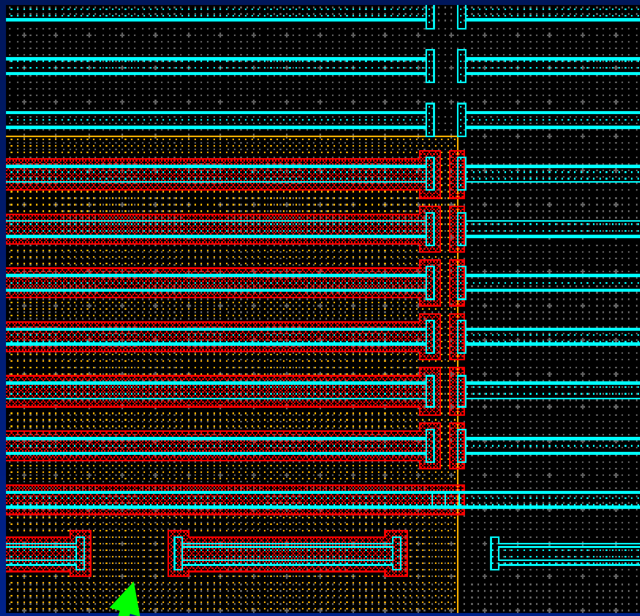
ΔCD/ Δ Flare



Flare map



Post-FVC

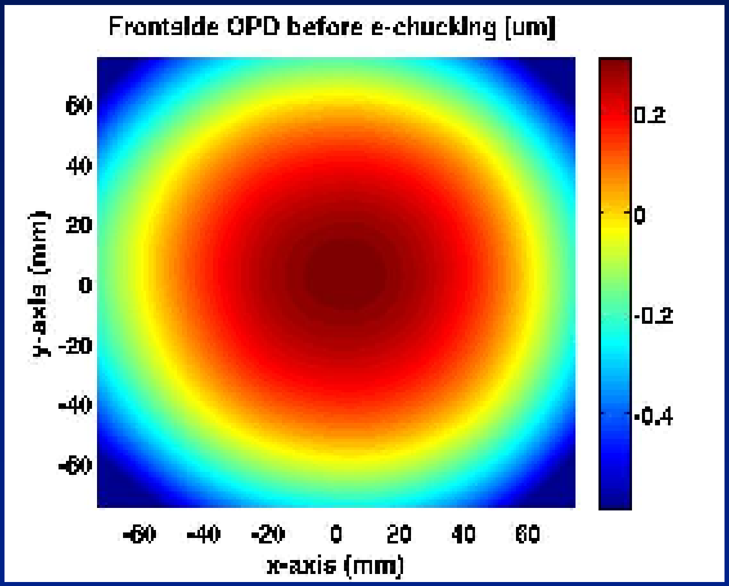


- All regions within the orange boundary get a bias depending on flare as per the equation below

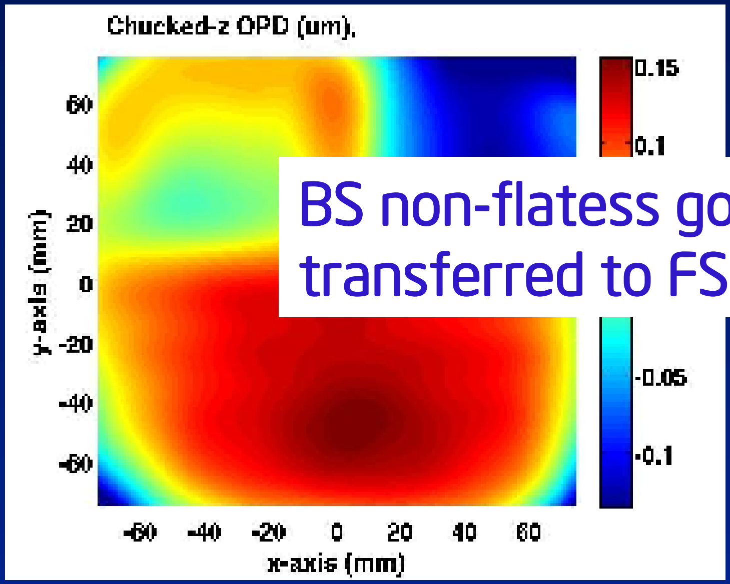
$$CD_{new} = CD_{drawn} + \frac{\partial CD}{\partial Flare}\Big|_{Flare_{local}} \times \left(Flare_{nominal} - Flare_{local}\right) / MEEF$$

Overlay error in EUV masks due to e-chuck

FS before e-chucking



FS after e-chucking

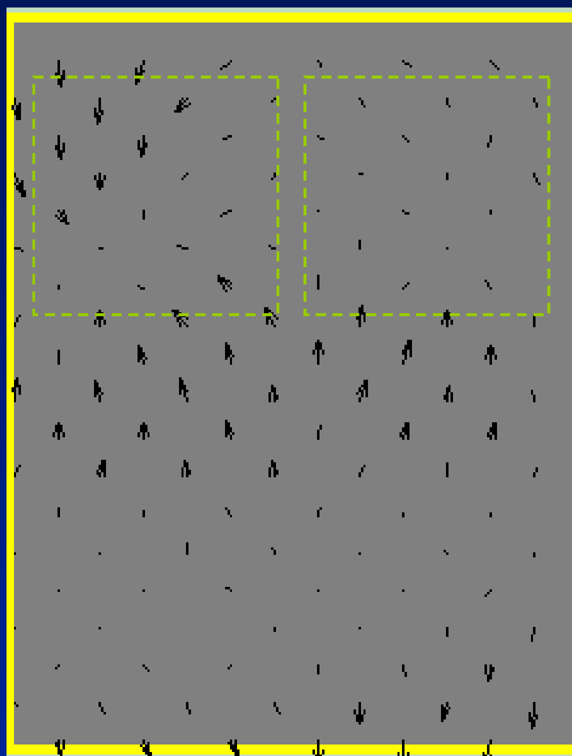


BS non-flatess got transferred to FS

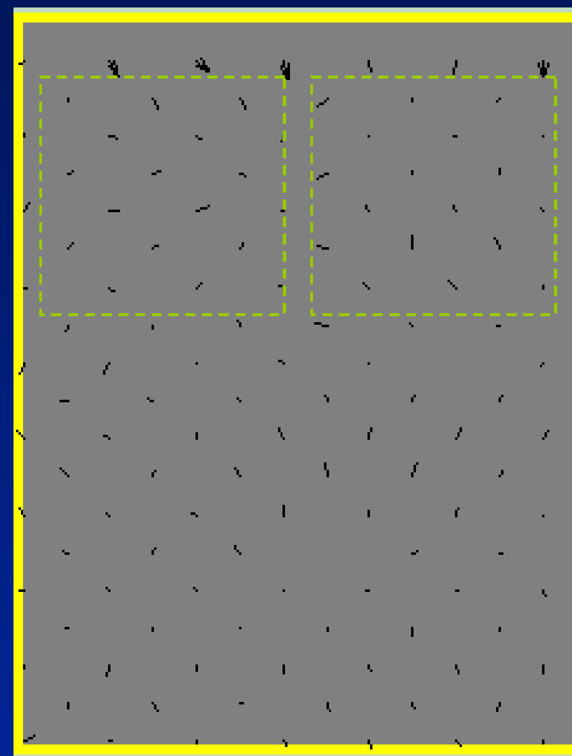
- Measure the FS & BS non-flatness of the mask
- Use a physically calibrated model of the e-chuck with the non-flatness data to compensate for OPD and IPD image placement errors using Ebeam Writer based Overlay error Correction (EWOC)

Mask non-flatness overlay data analysis

Uncompensated



Compensated



Residual 3sigma
X=3.6nm
Y=9.1nm

Residual 3sigma
X=4.3nm
Y=5.0nm

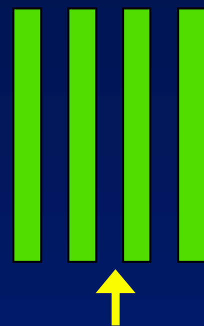
The compensated map shows improvement in overlay.

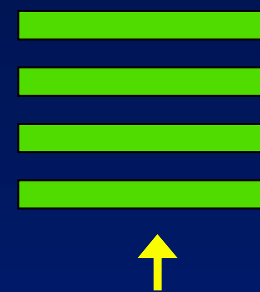
Reflective mask issues

Parallel

Perpendicular

Incident angle = 0°
Parallel

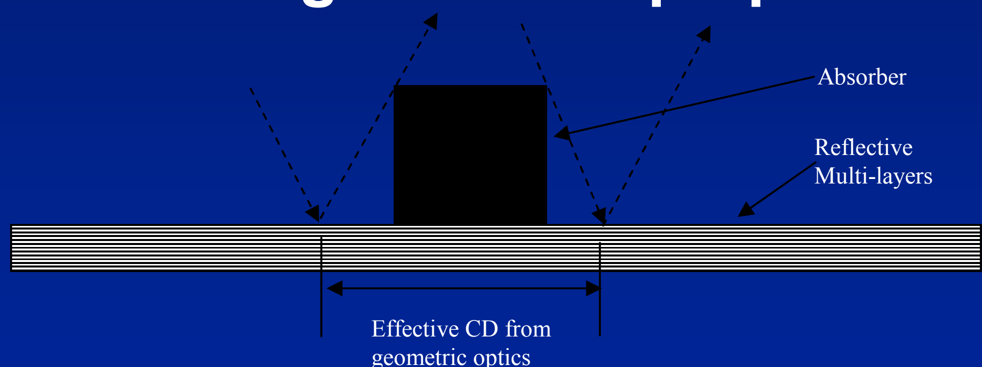




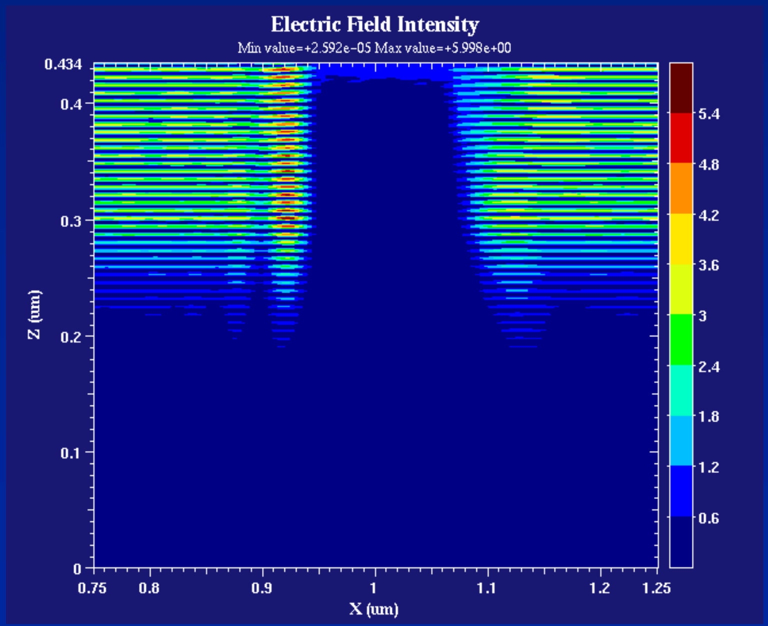
Incident angle = 6°
Perpendicular

Absorber height of ~ 51-87 nm

Shadowing effect for perpendicular



E-field at mask



Produces H-V bias, distorts 2D features

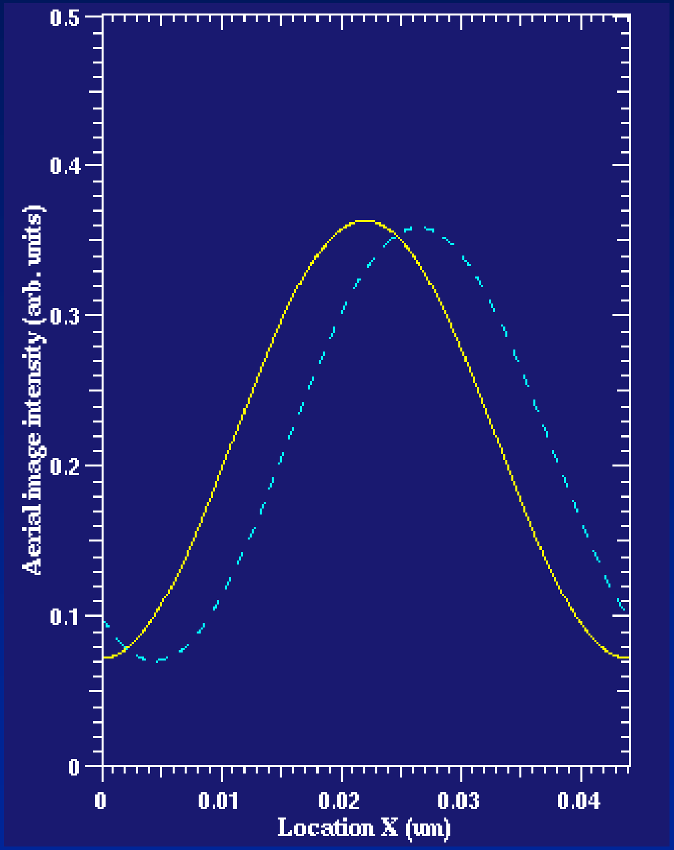
Center shift of “perpendicular” lines, contacts

Difference in best focus for H & V

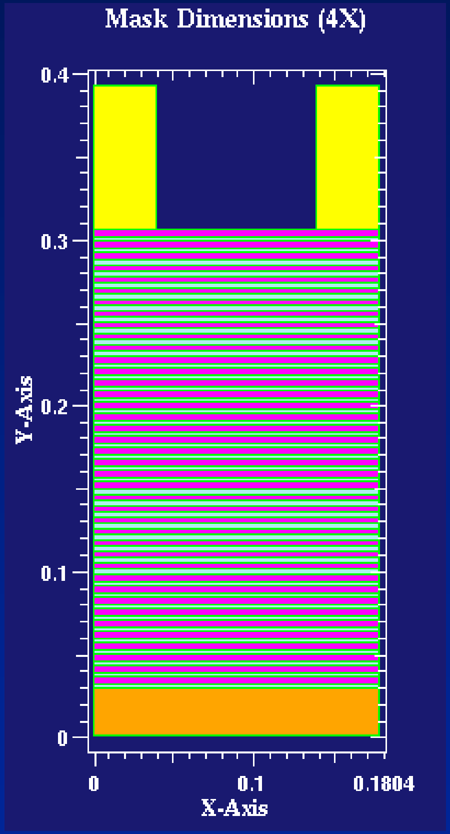
intel

22 nm hp full 3-D simulations with shadowing

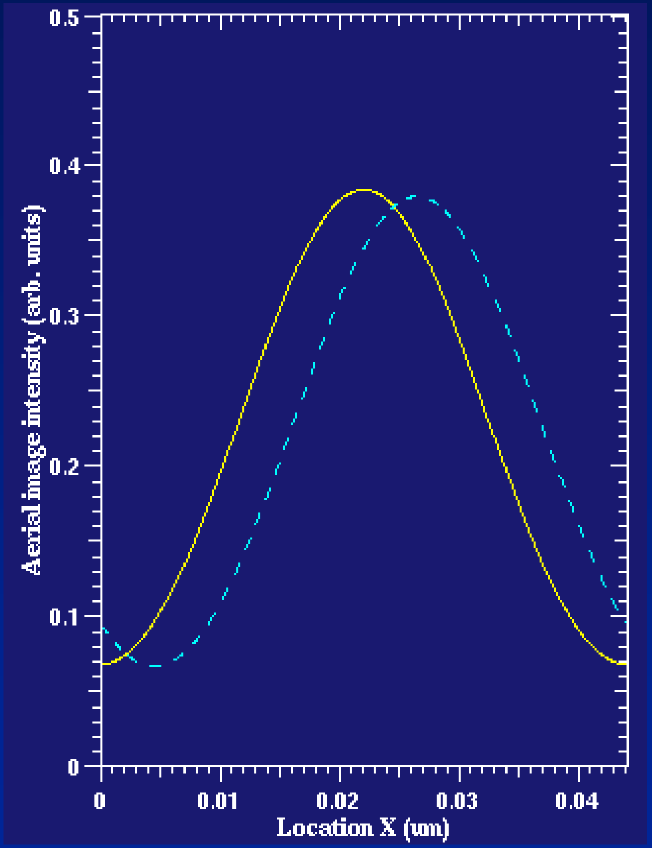
0.25 NA, OAI



Film Stack

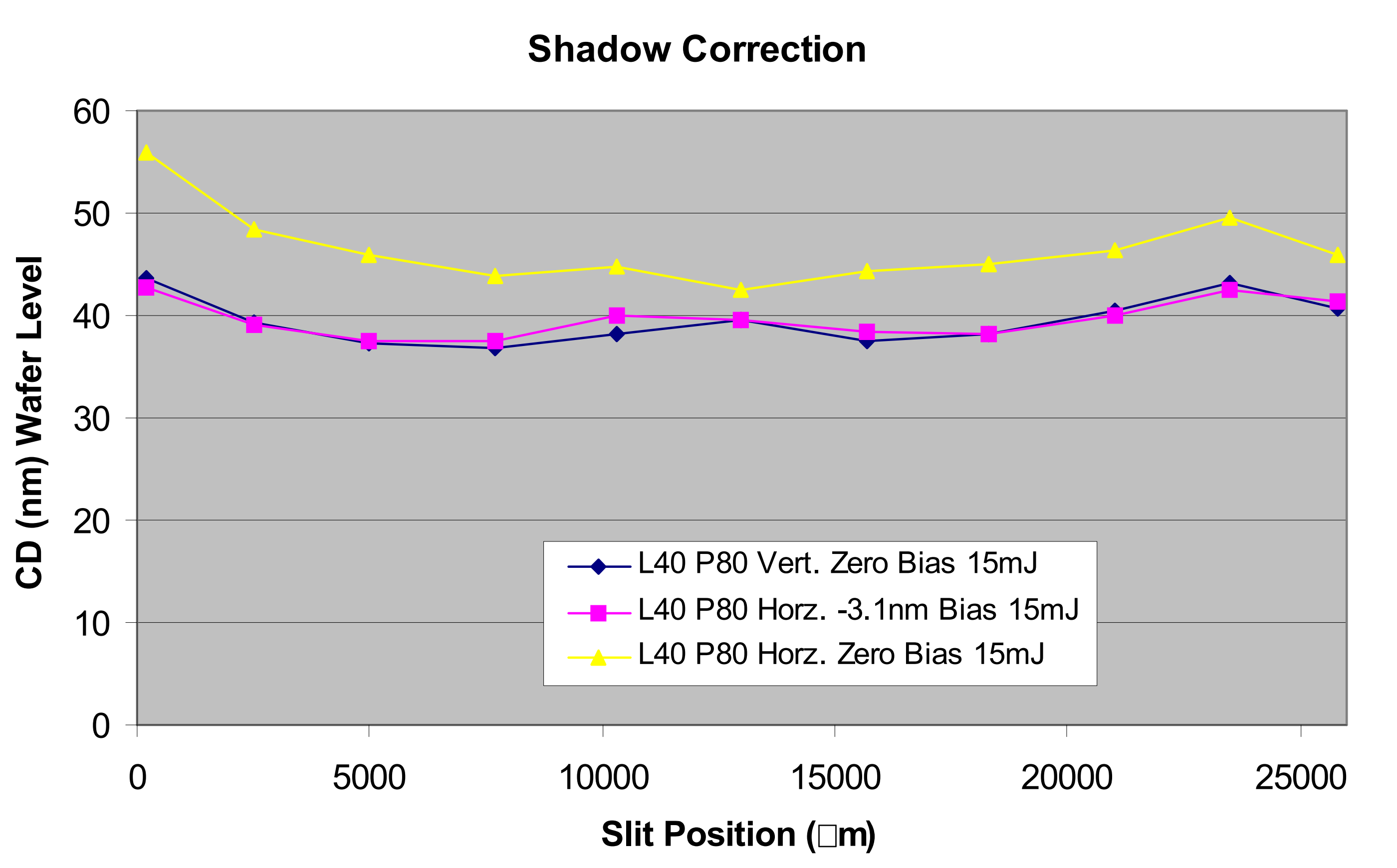


0.32 NA, disk



- Due to shadowing the mask CD for H trenches needs to be biased by 7 nm wrt vertical (for 87 nm absorber thickness)
- No degradation seen in DOF & MEEF for H spaces wrt V trenches for 0.25 NA

Mask Shadowing Compensation



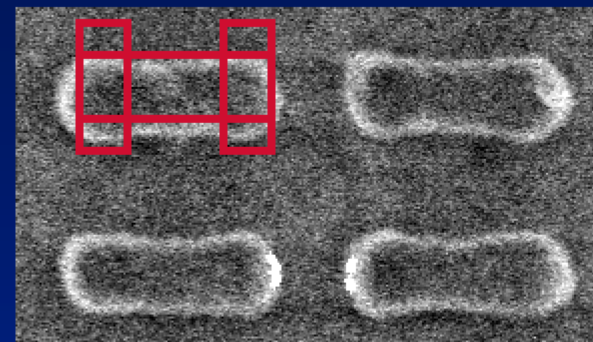
- Mask shadowing correction
  - Across slit variation will be compensated for based on Effective Shadowing Angle (ESA) variation across the slit
  - CD H bias of -3.1 nm makes H-V bias = 0

OPC is needed for EUV

0 nm hammerhead

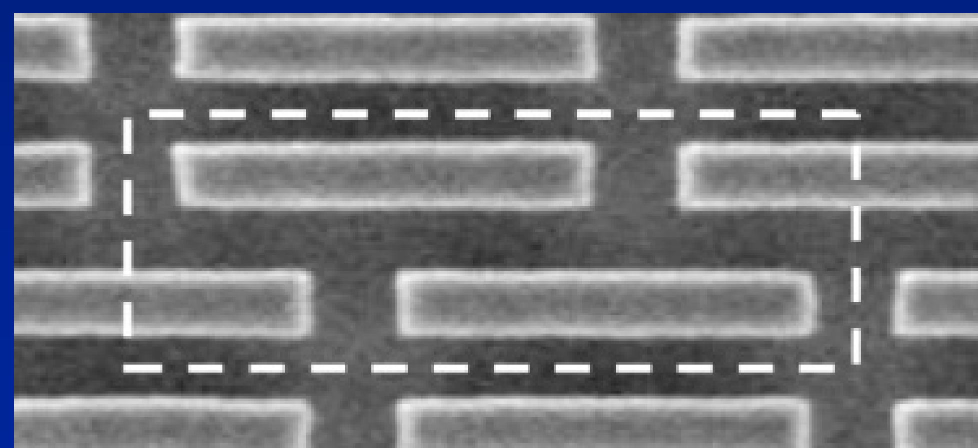
9 nm hammerhead

18 nm hammerhead



193 nm patterns set a high bar

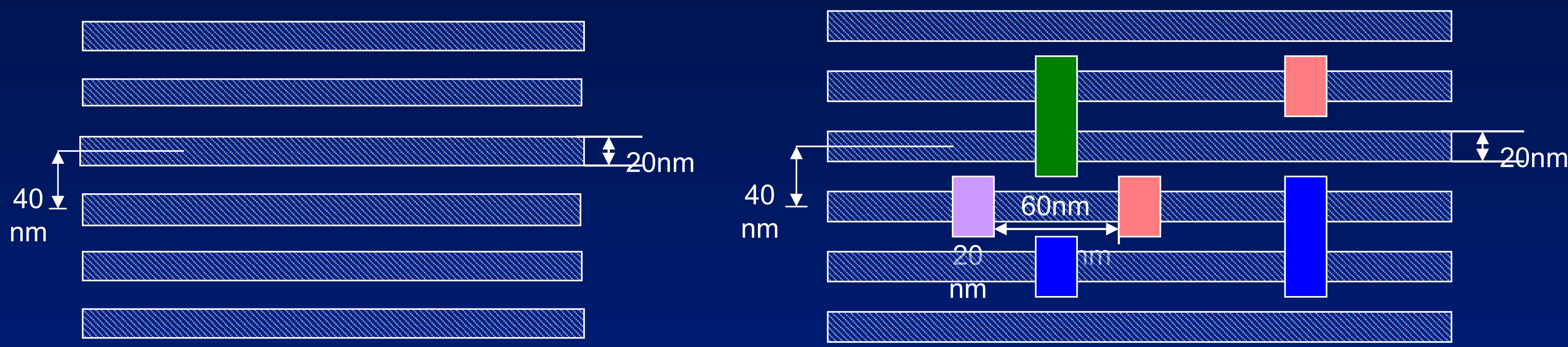
193 nm patterned gates



- OPC needed for
  1. Proximity bias
  2. Corner rounding
  3. ETE pull-back

11nm Logic Node*

ArF Only Patterning



1 193i w/PD to form gratings + 4 193i Masks/Exposures to form Pattern = 5 Mask
5 Exposures

Complementary Patterning

CD, LWR <2nm 3s

CD, LWR <4nm 3s

1 Mask/1 193i Expose + 1 Mask/1 EUV Expose or 0 Mask/1 EBDW Expose

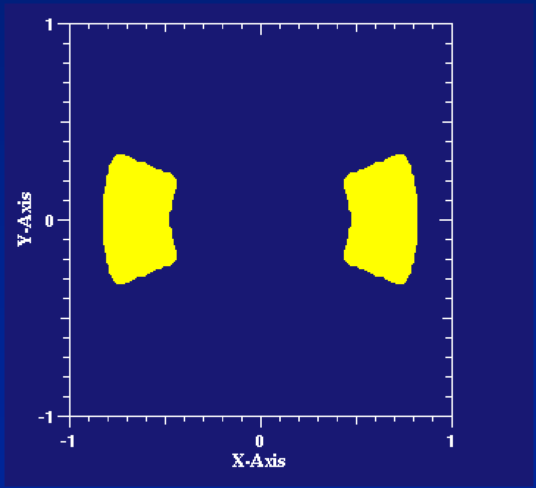
1 193i w/PD to form gratings + 1 EUV Masks/Exposure or 0 Mask/1 EBDW Exposure

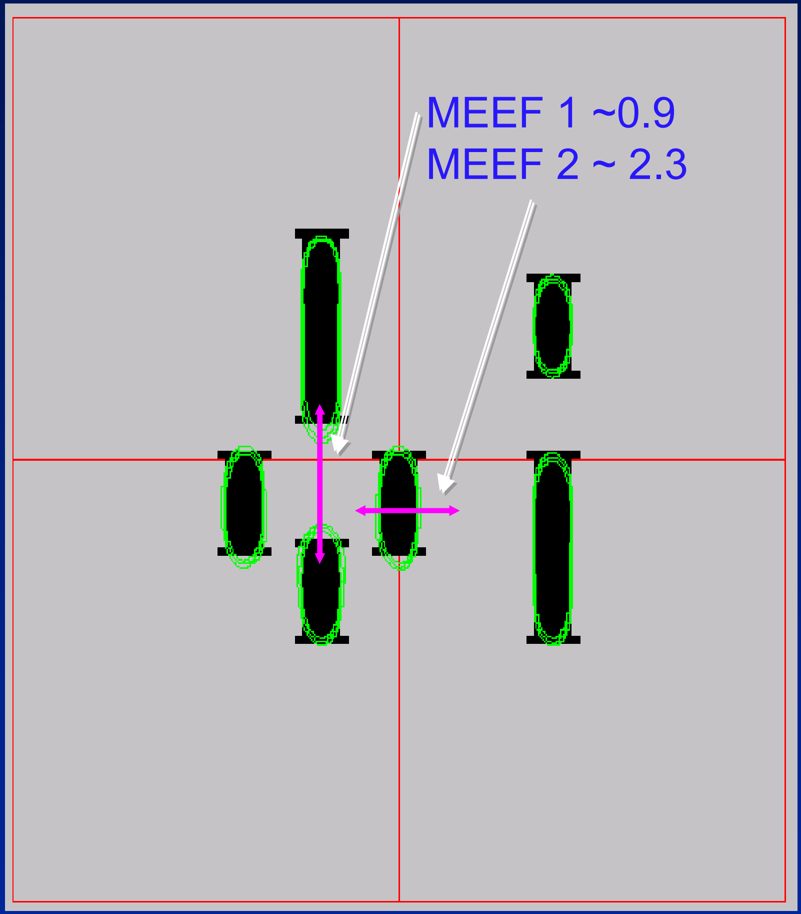
Total 2 Masks/2 Exposures or 1 Mask/2 Exposures

*Y. Borodovsky, 2010 KLA Tencor Litho User Forum

Learning for 11nm node 193i+EUV Complementary can start in 2011 with 0.25NA*

Wavelength = 13.5 nm, NA = 0.25
Illumination: C-Dipole 0.5/0.8
Flare = 4.5% (assuming tool flare = 6% and 25% dark density)
Clear area reflectivity = 65%
Dark area reflectivity = 0.9%
Acid Diffusion =7.5nm





NA > 0.30 will allow use of less restrictive illumination in 2012 for 11nm node DR development

*Y. Borodovsky, 2010 KLA Tencor Litho User Forum

Summary

- While challenges remain for introduction into HVM, tremendous savings in complexity for 22 nm hp patterns can be achieved by using EUVL
- 22n hp patterning needs using EUVL have been identified on several fronts
  - OAI for 0.25 NA
  - LWR, Esize, and diffusion length improvement in photoresist
  - Compensations for optical proximity effects, flare, mask shadowing, and mask non-flatness

Acknowledgements

- Steve Putna, Todd Younkin, Grant Kloster, Alan Myers, Guojing Zhang, Seh-Jin Park, Ted Liang, Pei-Yan Yang, Michael Leeson, Sang H. Lee, Yash Shroff, Uday Shah, Willy Rachmady, Gilroy Vandentop, Charlie Wallace, Chris Kenyon, Rich Schenker, Yan Borodovsky, Sam Sivakumar, Steve Carson
- UC, Berkeley
- IMEC
- SEMATECH

Back up

nZ(22) = Quantitative Resist Comparison

$$Z\text{-}FACTOR^{1}\ (mJ^{*}nm^{3}) = (RES)^{3} * (LER)^{2} * (SEN)$$

$$nZ_{22} = \frac{\text{Material Z-Factor}}{\text{22 HP Target Z-Factor}}$$

	CD (nm)	MIN LWR 3s (nm)	ESIZE (mJ/cm2)	Z-FACTOR (mJ*nm3)	nZ_{22}	nZ_{32}
22 HP Target	22	1.20	10.00	7.7E-10	1.0	0.1
32 HP Target	32	2.00	10.00	6.6E-09	8.5	1.0
2009 Goal	22	4.00	12.50	1.1E-08	13.9	1.6
2010 Goal	22	3.00	11.30	5.4E-09	7.1	0.8

PRO

- Simplified approach where limiting resolution (RES) is proxy for resist blur / diffusion length…
- Quick, easy to calculate, quantifies improvement, plugs into infrastructure…

CON

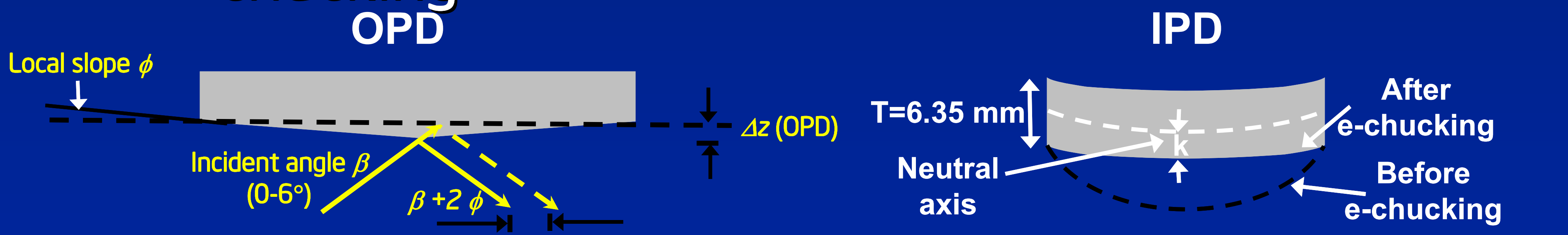
- Simplification results in exposure-tool / illumination-dependent Z-factor since NILS is not accounted for…
- Determination of RES, LER, or SEN can be user specific…

Intel Benchmarking All EUV Resists Using nZ_{22} Moving Forward

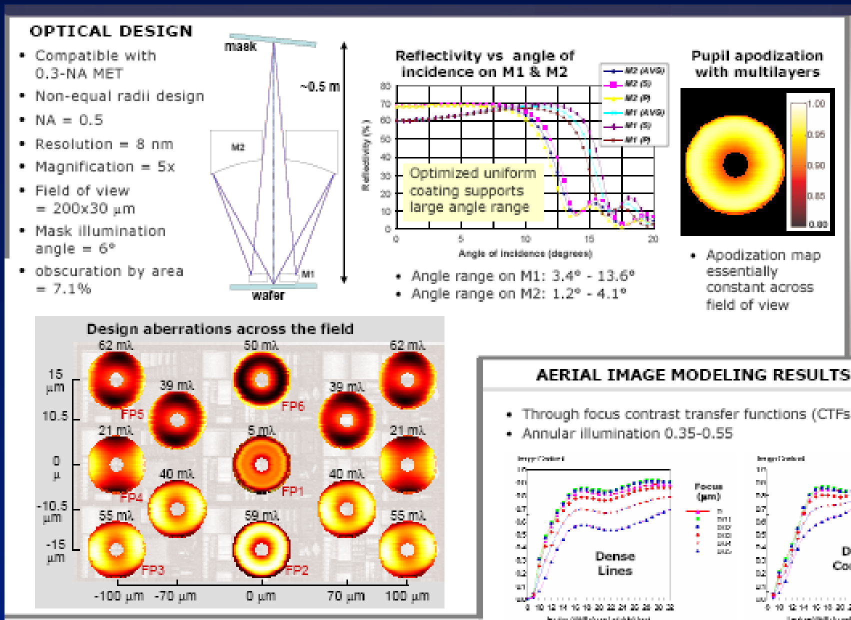
[1]Wallow, et al SPIE 69211F (2008)

Overlay error in EUV masks due to e-chuck

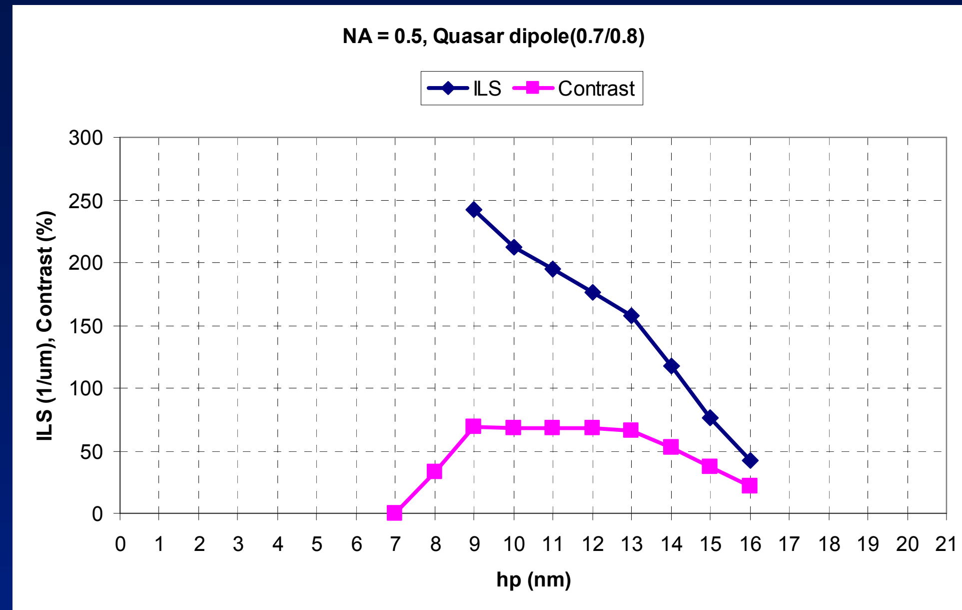
- Due to off-normal angle of incidence, EUV systems are non-telecentric on mask side, so Out of Plane Distortion (OPD) or Δz height variation of the mask plane results in pattern shift
- In Plane Distortion (IPD) Pattern shift due to FS shape (local slope) change on mask after e-chucking

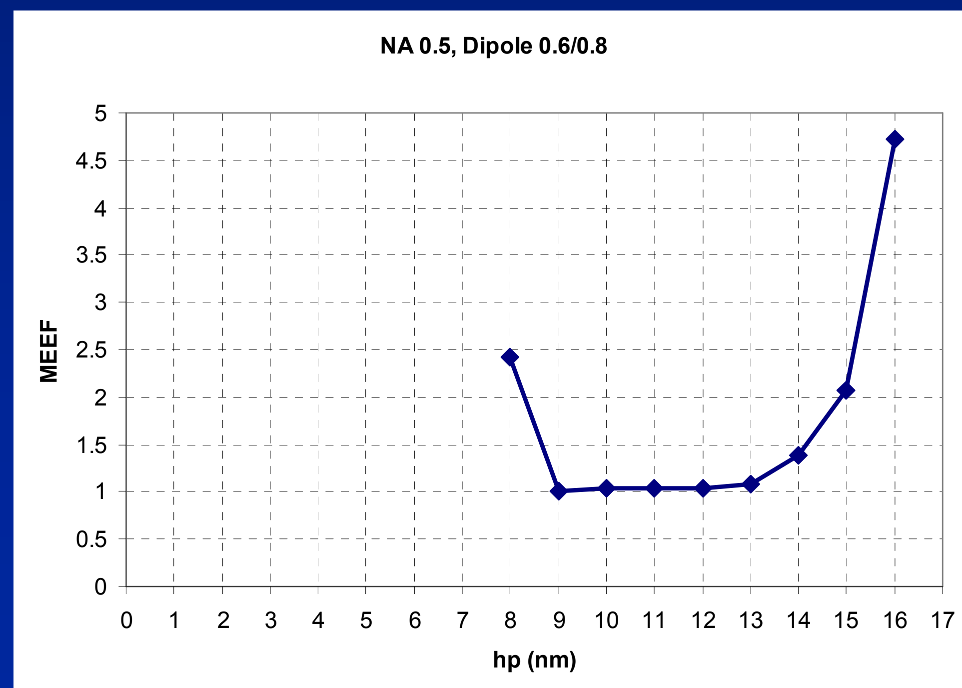


"MET2" NA 0.5, outer sigma max 0.8



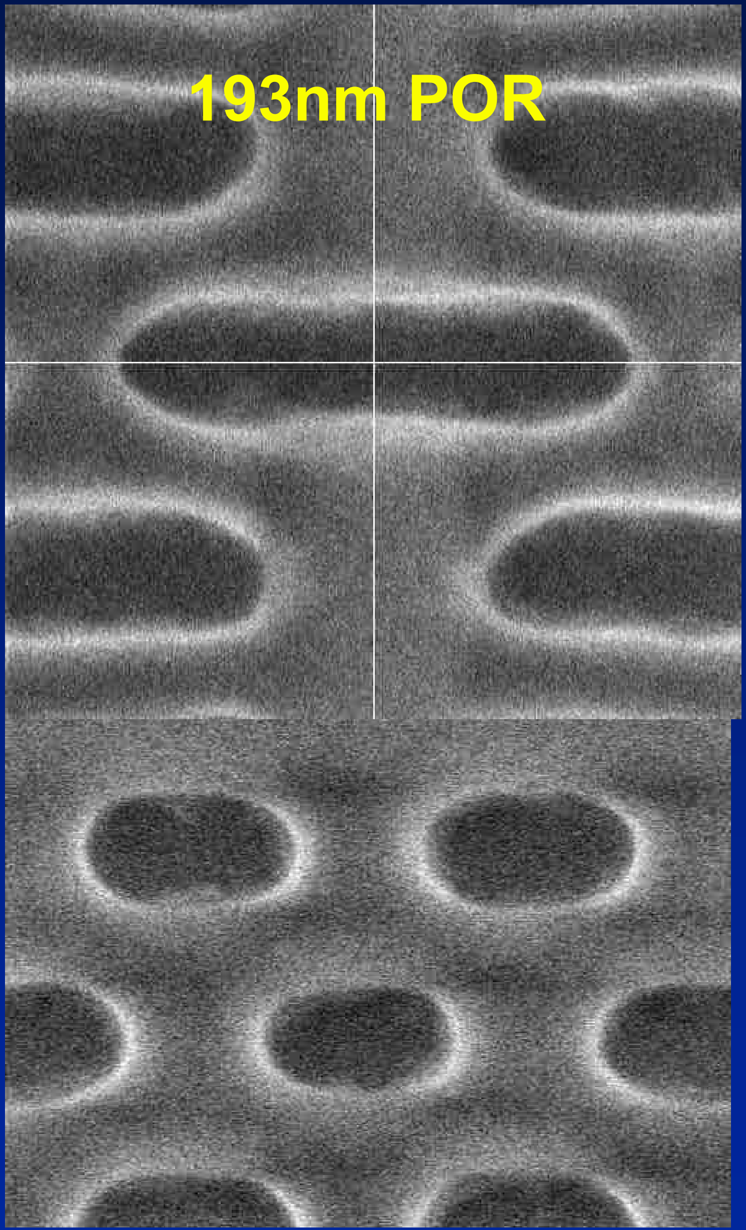
P. Naulleau, M. Goldstein, R. Hudyma, 2008 EUVLS
M. Goldstein et al, Optics Letters, Vol 33, No. 24, Dec. 15, 2008

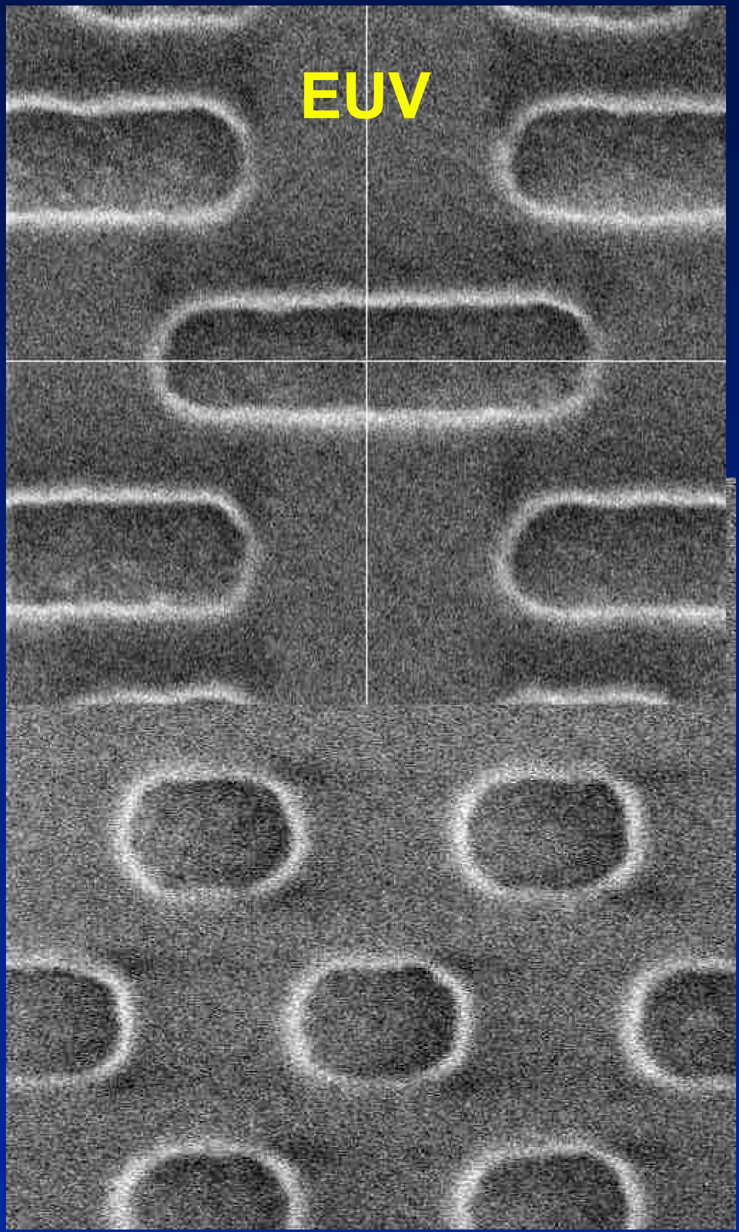




- Ultimate resolution using dipole ~ 9 nm
- 9 nm hp: MEEF ~1, Contrast = 69%, ILS ~250
- Note: Smaller poles can decrease uhp

Staggered trenches 112.5 nm pitch





- Less corner rounding with EUV

EUV Litho - Key Gaps*

*S. Sivakumar (Intel), Lithovision (2009)

1. Source readiness: funded by suppliers
2. Zero defect reticle process capability: funded by Intel and was 2009 internal focus
3. EUV AIMS and 3G blank inspection: not funded (cost ~ $150M [illegible] industry enabling [illegible])

BIG ISSUES REMAIN

4. Blank defect improvement trend: insufficiently funded by suppliers (cost is unknown ~ $50M)
5. Fab reticle quality control infrastructure: not funded (cost ~ $10M single tool cost)

Technical gaps, especially on the mask defectivity and inspection fronts, will limit EUV HVM insertion if not addressed in time

intel